Claims

1. An interface for transferring data from a real-time data transfer system to a signal processing unit comprising:

a circular buffer having an input configured to receive data samples from the real-time data transfer system and to periodically send data samples received from the real-time data transfer system to the signal processing unit when the signal processing unit accepts a transfer, wherein the data is stored and transferred according to a first-in, first-out operational protocol; and

a first counter circuit communicating with the signal processing unit and the data transfer system and configured to increment for each data sample sent to the circular buffer from the data transfer system and decrement for each data sample sent to the signal processing unit from the circular buffer, where the counter circuit is configured to count beyond the physical range of the buffer to account for data samples transferred through the circular buffer.

2. An interface according to Claim 1, wherein the counter circuit has a programmable threshold and is configured to generate an interrupt to the signal processing unit when the counter passes the threshold.

3. An interface according to Claim 2, wherein the counter is configured to send a subsequent interrupt only after a prior interrupt is acknowledged by the signal processing unit.

4. An interface according to Claim 1, wherein the signal processing unit polls the counter periodically to determine the availability of data samples.

5. An interface according to Claim 1 further comprising:

a second circular buffer having an input and an output configured to receive data samples from the signal processing unit and to send data samples to the real-time data transfer system when the data is available; and

a second counter circuit communicating with the second circular buffer and configured to increment each time a data sample is received by the second circular buffer from the signal processing unit and decrement each time a data sample is sent from the second circular buffer to the data transfer system, where the counter is configured to count beyond the physical range of the buffer.

6. An interface according to claim 5, further comprising:

a switch communicating with the second counter circuit and the data transfer system; and

a null signal generator communicating with the switch for sending a null signal to the data transfer system when a second threshold has been reached.

7. An data transfer device for transferring data from a data transfer system to a signal processor comprising:

buffer means configured to store and transfer data samples between the data transfer system and the processor in a synchronized manner, such that the number of receive samples transferred is substantially equal to the number of transmit samples transferred;

counter means configured to account for data transferred through the buffer means, where the counter means is further configured to count beyond the physical length of the buffer.

8. An interface according to Claim 7, wherein the counter means includes interrupt means configured to send a signal to the signal processor when the counter means increments beyond a first threshold, to receive an acknowledgment signal from the signal processing unit to acknowledge an interrupt signal sent by the counter means and to send a subsequent a interrupt signal only after a prior interrupt signal has been acknowledged.

9. An interface according to Claim 7, wherein the signal processor periodically polls the counter means to determine the availability of data samples.

10. A modem for communicating on a data transfer system comprising:

a signal processor for processing data;

means for converting an analog signal received by the buffer to an digital signal readable by the processor and vice versa;

buffer means configured to store and transfer data samples between the data transfer system and the processor in a synchronized manner, such that the number of receive samples transferred is substantially equal to the number of transmit samples transferred; and

counter means configured to account for data transferred through the buffer means to the signal processor , where the counter means is further configured to count beyond the physical length of the buffer.

11. An modem according to Claim 10 further comprising means for sending a null signal when data is not ready to be transferred from the buffer means to the data transfer system.

12. An modem according to Claim 10, wherein the most significant bit of the counter means is a sticky bit and is configured to retain a digital logic one in the event of an overflow of the counter and is configured to lose the digital logic one when the counter is subsequently decremented as a result of the signal processing unit reading data from the first buffer means.

13. An interface for transferring data between a signal processing unit and a data transfer system comprising:

a buffer circuit configured to transfer data samples between a data transfer system and a signal processing unit in synchronicity, the buffer circuit having at least one input for receiving data samples and at least one output for transmitting data samples, wherein the data samples are transferred according to a first-in, first-out protocol;

at least one counter circuit communicating with the signal processing unit and the data transfer unit to count the number of data samples transferred from each circular buffer, where the counter circuit is configured to count beyond the physical range of the buffers; and

an interrupt circuit communicating between the counter circuit and the signal processing unit to transmit an interrupt signal to the data processing unit when the counter reaches a predetermined threshold to indicate that the buffer has a minimum number of samples available for processing.

14. An interface according to claim 13 further comprising:

a null signal generator communicating with the counter;

a switching circuit communicating with the counter circuit, with the data transfer system, with the null signal generator and with a first output of the buffer circuit for alternating communication between the data transfer system and the first output of the buffer circuit and between the data transfer system and the null signal generator to transfer data from the buffer circuit to the data transfer system when data is available and to transfer a null signal from the null signal generator to the data transfer system when data is not available.

15. A method of transmitting a communications signal between a host signal processor (HSP) and a data transfer system comprising:

receiving an analog signal generated in compliance with a communication standard protocol;

converting the analog signal to a digital data signal representing digital data samples;

storing the digital data samples to a receive buffer according to a first-in, first-out operational protocol;

transmitting the digital data samples from the receive buffer to the HSP according to the first-in, first-out operational protocol;

storing second digital data samples in a transmit buffer according to a first-in, first-out operational protocol; and

transmitting the digital data samples from the transmit buffer according to the first-in, first-out operational when digital data is available;

synchronizing the transmit and receive buffers such that the number of new samples avaible in the receive buffer for reading by the HSP is equal to the number of sample spaces in the transmit buffer available for writing by the HSP; and

counting the number of samples in the buffers such that the counting mechanism has a range greater than the physical size of the buffers.

16. A method according to Claim 15 wherein the digital data samples are transmitted from the receive buffer to a host signal processor (HSP), wherein an interrupt signal is transmitted to the HSP to indicate when the buffer contains a predetermined amount of data.

17. A method according to Claim 15 further comprising transmitting a null signal when digital data samples are not available